REMARKS

Claims 1-12 remain pending in the application. Claims 1, 4 and 8 are amended. Reconsideration of the rejection and allowance of the pending application in view of the following remarks are respectfully requested.

In the Office Action, the Examiner rejected claims 1, 2, 4-6 and 8-10 under 35 U.S.C. §102(e) as being anticipated by Nagase (U.S. Patent No. 7,046,293).

Applicant's claim 1, as currently amended, recites a method of reducing a power supply voltage which is supplied from a voltage regulator to at least one particular circuit. The voltage regulator is configured to adjust its output voltage by use of an external output voltage setting circuit connected thereto. A switching element is used to connect an output voltage setting terminal of the voltage regulator to a ground via a predetermined resistance. The method includes, inter alia, turning off the switching element so that the output voltage of the voltage regulator is set at a preset power supply voltage. The preset power supply voltage is a function of resistance values of the external output voltage setting circuit. The method also includes turning on the switching element so that the output voltage of the voltage regulator is reduced to a predetermined voltage which is lower than the preset power supply voltage. The predetermined voltage is a function of resistance values of the external output voltage setting circuit.

Applicant's claim 4, as currently amended, recites a power supply voltage reduction system for reducing a power supply voltage which is supplied to at least one particular circuit from a voltage regulator which includes, inter alia, an output voltage setting circuit that is connected to the voltage regulator to adjust an output voltage of the voltage regulator, a switching element, and a controller that controls an on/off state of the

switching element. The controller switches the switching element to one of the on and off states so that the output voltage of the voltage regulator is reduced to a predetermined voltage which is lower than a preset power supply voltage. The predetermined voltage and the preset power supply voltage are functions of resistance values of the output voltage setting circuit.

Applicant's claim 8, as currently amended, recites a CCD driving system which includes, inter alia, a CCD driving circuit, a timing generator, a voltage regulator that supplies a preset power supply voltage to the CCD driving circuit and the timing generator, an output voltage setting circuit that is connected to the voltage regulator to adjust an output voltage of the voltage regulator, a switching element, and a controller that controls an on/off state of the switching element. The controller switches the switching element to one of the on and off states so that the output voltage of the voltage regulator is reduced to a predetermined voltage which is lower than a preset power supply voltage. The predetermined voltage and the preset power supply voltage are functions of resistance values of the output voltage setting circuit.

Nagase discloses a power supply circuit 10 which includes a micro-computer 18, a power switch 20, a switching controller 22, a first terminal 24a, a second terminal 26a, and a short-circuit 28 which includes resistors R1-R5, a transistor Q3 and a FET Q2. See Fig. 1 of Nagase. In response to turning-on the power supply switch 20, the micro-computer 18 outputs a power-on signal, the switching controller 22 outputs 15V to the first terminal 24a and -7.5V to the second terminal 26a, and the transistor Q3 and the FET Q2 are turned off. See col. 4, lines 41-53 of Nagase.

In response to turning-off the power supply switch 20, the micro-computer 18 outputs a power-off signal, the 15 V voltage at the first terminal 24a and the -7.5 V voltage at the second terminal 26a are shut off, and the transistor Q3 and the FET Q2 are turned on. See col. 4, line 53 – col. 5, line 2 of Nagase. This causes the short-circuit 28 to operate so that the first terminal 24a and the second terminal 26a are short-circuited together, and the residual charges at the first terminal 24a and the second terminal 26a decrease to 0. See col. 5, lines 2-18 of Nagase.

In the Office Action, the Examiner asserts that the voltage at the first terminal 24a is a voltage regulator output voltage.

Applicant respectfully submits that the voltage at Nagase's first terminal 24a is not a function of resistance values of the short-circuit 28. Rather, when the power supply switch 20 is on (and the transistor Q3 and FET Q2 are off), 15 volts is outputted to the first terminal 24a, independent of resistances values R1-R5 of the short-circuit 28. Further, when the power supply switch 20 is off (and the transistor Q3 and FET Q2 are on), the first terminal 24a and 26a are shorted together, and the residual charge at the first terminal 24a decreases to 0 V, independent of the resistance values R1-R5. That is, the voltage values of 15 V and 0 V, which are outputted at the first terminal 24a, are not functions of any of the resistance values R1-R5 of the short-circuit 28.

Thus, Applicant submits that Nagase fails to disclose or suggest a method of reducing a power supply voltage which includes turning off a switching element so that an output voltage of a voltage regulator is set at a preset power supply voltage, and turning on the switching element so that the output voltage of the voltage regulator is reduced to a predetermined voltage, where the preset power supply voltage and the

predetermined voltage are functions of resistance values of an external output voltage setting circuit connected to the voltage regulator, as recited in Applicant's amended claim 1.

Similarly, Nagase also fails to disclose or suggest a power supply voltage reduction system which includes a controller which switches a switching element to one of an on and an off state so that an output voltage of a voltage regulator is reduced to a predetermined voltage which is lower than a preset power supply voltage, where the predetermined voltage and the preset power supply voltage are functions of resistance values of an output voltage setting circuit connected to the voltage regulator, as recited in Applicant's claim 4.

Further, Nagase fails to disclose or suggest a CCD driving system which includes a controller which switches a switching element to one of an on and an off state so that an output voltage of a voltage regulator is reduced to a predetermined voltage which is lower than a preset power supply voltage, where the predetermined voltage and the preset power supply voltage are functions of resistance values of an output voltage setting circuit connected to the voltage regulator, as recited in Applicant's claim 8.

For at least these reasons, Applicant submits that the inventions recited in Applicant's independent claims 1, 4 and 8 are not anticipated by Nagase, and requests that the Examiner withdraw the 35 U.S.C. §102(b) rejection and allow claims 1, 4 and 8.

Applicant submits that claim 2, 5, 6, 9 and 10 are also in condition for allowance, in view of their dependency from claims 1, 4 and 8.

In the Office Action, the Examiner rejected claims 3, 7 and 11 under 35 U.S.C. §103(a) as being unpatentable over Nagase in view of Kondo (U.S. Patent No.

5,600,521). Applicant respectfully submits that Kondo fails to overcome the above-noted deficiencies of Nagase. Thus, Applicant submits that the inventions recited in independent claims 1, 4 and 8 are not obvious in view of the combined teachings of Nagase and Kondo, and respectfully requests withdrawal of the 35 U.S.C. §103(a) rejection of claims 3, 7 and 11, which depend from claims 1, 4 and 8.

Based on the above, it is respectfully submitted that this application is in condition for allowance, and a Notice of Allowance is respectfully requested.

SUMMARY AND CONCLUSION

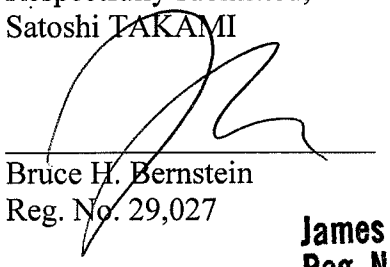
Reconsideration of the outstanding Office Action, and allowance of the present application and all of the claims therein are respectfully requested and believed to be appropriate. Applicant has made a sincere effort to place the present invention in condition for allowance and believes that he has done so.

Any amendments to the claims which have been made in this amendment, and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

Should an extension of time be necessary to maintain the pendency of this application, including any extensions of time required to place the application in condition for allowance by an Examiner's Amendment, the Commissioner is hereby authorized to charge any additional fee to Deposit Account No. 19-0089.

Should the Examiner have any questions or comments regarding this response, or the present application, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
Satoshi TAKAMI



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